REMARKS

This Response is intended to be fully responsive to the Office Action dated February 24, 2006. In view of the following discussion, the Applicants believe that all claims are presently allowable.

DRAWING OBJECTIONS

Figure 3 stands objected to as showing only prior art without being labeled as such. The Applicants respectfully disagree.

The Examiner is mistaken that Figure 3 depicts a common, commercially available CENTURA® semiconductor wafer processing system. Paragraph 30, cited by the Examiner, merely states that the process may be performed in an etch module of the CENTURA® system. The detailed description with respect to Figure 3 depicts a schematic diagram of an etch reactor "that illustratively may be used to practice portions of the invention" and that generally may be used as a processing module of the CENTURA® system. (*See, Application*, [0044] *et seq.*)

The etch reactor 302 depicted in Figure 3 includes a process chamber 310 and a controller 340, having the inventive method stored therein as a software routine 304. (*Id.*, [0052]-[0053].) Accordingly, the etch reactor depicted in Figure 3 includes structure differing from the prior art. Thus, Figure 3 should not be labeled "Prior Art," as requested by the Examiner.

Thus, the Applicants submit that Figure 3 is proper. Accordingly, the Applicants respectfully request that the objection be withdrawn.

CLAIM REJECTIONS

A. Claims 1-6, 8-10 and 40-45

Claims 1-6, 8-10 and 40-45 presently stand rejected as being unpatentable over United States Patent No. 6,797,633, issued September 28, 2004, to *Jiang, et al.* (hereinafter *Jiang*) in view of United States Patent Application Publication Serial No. 2004/0161930, published August 19, 2004 to *Ma, et al.* (hereinafter *Ma*), and/or United States Patent No. 6,797,633, issued July 30, 2002 to *Ikeda* (hereinafter *Ikeda*). The Applicants respectfully disagree.

Independent claims 1 and 40 recite limitations not taught or suggested by any combination of the cited references. *Jiang* describes a method for forming a dual damascene trench patterning method. However, *Jiang* fails to teach or suggest etching in-situ the cap layer, a trench in the second dielectric layer, the masking material, and the second barrier layer, by providing a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts while etching, as recited in claim 1, or supplying a source power of at least about 1000 Watts at a frequency of above about 100 MHz to the plasma source electrode and a bias power of at least about 800 Watts to the substrate bias electrode while etching the dielectric layer as recited in claim 40.

Ma discloses a method of *in-situ* discharge prior to a plasma etch in order to avoid arcing within the chamber during the plasma etch process. (*Ma*, paragraph [0001].) *Ma* further discloses applying an RF power in the range of 100 to 1000 Watts for a 200 mm wafer and from 100 to 2000 Watts for a 300 mm wafer. (*Ma*, paragraph [0028].) However, *Ma* is silent regarding the bias power applied. As such, *Ma* fails to teach or suggest a modification of *Jiang*, alone or in combination with any of the other cited references, that would yield a plasma source power of at least 1,000 Watts and a bias power of at least about 800 Watts while etching during at least a portion of the etch step, as recited in claims 1 and 40.

Moreover, although the Examiner contends that it would have been obvious to modify the etch steps of *Jiang* using the power, pressure, and flow rates as taught by the discharge sequence of *Ma* in order to avoid arcing during the plasma etch processes, *Ma* discloses that the discharge sequence is performed prior to the plasma etch process. (*Ma*, paragraph [0014]). Specifically, *Ma* states that no etching of the photoresist layer or substrate occurs during the discharge sequence. (*Ma*, paragraph [0028]). As such, *Ma* fails to teach or suggest any combination that results in providing these conditions while etching, as recited in claims 1 and 40. Accordingly, any combination of *Ma* and *Jiang* would result in a method wherein a discharge step that does not etch the substrate would be performed prior to plasma etching in order to avoid arcing.

Thus, there is no suggestion to modify the etch steps of *Jiang* with the process conditions of the discharge sequence taught by *Ma*, in a manner that would yield the limitations recited in claims 1 and 40.

In the Response to Amendment section of the Office Action dated February 24, 2006, the Examiner states that "although not taught as a preferred embodiment, Ma teaches this embodiment nonetheless…." The Applicants respectfully disagree. Contrary to the Examiner's assertion, *Ma* does not make a broad disclosure relating to bias and power conditions and then limit such disclosure to a "preferred embodiment" wherein the substrate is not etched during the discharge sequence. The only disclosure in *Ma* relating to the claimed power condition is in connection with the discharge sequence in which it is clearly stated that no etching occurs. Accordingly, and as noted above, *Ma* fails to teach or suggest providing the claimed bias and power conditions while etching, as recited in claims 1 and 40.

The Examiner also refers, in the Response to Amendment section, to a statement in the Abstract of *Ma* to assert motivation to modify the teachings of *Jiang*. Specifically, the Examiner points to the statement in *Ma* that "the method is extendable to etching low K dielectric layers." However, this statement merely reflects the fact that the discharge sequence may be performed at various stages throughout fabrication. For example, the Summary of the Invention section states that the discharge sequence may be beneficial when "etch transferring a pattern into a low k dielectric layer that has a poor thermal conductivity and tends to produce arcing in conventional etch processes." (*Ma*, ¶[0016].) The teaching to use the discharge sequence (during which *Ma* teaches that no etching occurs) prior to etching a low k dielectric layer does not supply any teaching, suggestion, or motivation to provide a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts while etching, as recited in claims 1 and 40. Accordingly, *Ma* fails to teach or suggest modifying the cited references in the manner asserted by the Examiner.

Ikeda discloses a method of manufacturing a semiconductor device wherein multiple etch steps are provided for etching different layers formed on a

substrate. One step of the etch process provides 1600W of electricity to an upper electrode and 1400W of electricity to a lower electrode. The Examiner asserts that it would have been obvious to modify *Jiang* with the power, pressure, and flow rates as taught by *Ikeda* to "reduce the F radicals which form a hardened surface layer." (Final Office Action dated August 8, 2005, p. 6, ll. 3-11; Office Action dated February 24, 2006, p. 5, ll. 8-16.) The Applicants respectfully disagree.

Ikeda provides no suggestion or motivation to modify the etch process as taught by *Jiang* (alone or modified by *Ma*) in a manner that yields the limitations recited in claims 1 and 40 because, contrary to the Examiner's assertion, *Ikeda* fails to teach or suggest providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts, as recited in claims 1 and 40, to reduce F radicals in the process chamber. To provide the benefit that the Examiner cites (*i.e.*, "to reduce F radicals which form a hardened surface layer"), *Ikeda* teaches that, in a parallel plate plasma etcher, "the upper electrode 703 is made of Si, which has high reactivity for F radicals. That is, the excessively generated F radicals are trapped by Si of the upper electrode so that F radicals are reduced." (*Ikeda*, col. 2, ll. 40-44.)

In addition, *Ikeda* teaches that sputtered Si from the upper electrode may deposit on the photoresist and form a hardened resist surface layer. *Ikeda* further teaches that the electricity to the upper electrode should be removed – *i.e.*, the upper electrode should be grounded – to cause a reduction in excess Si atoms which prevents the hardened surface layer from being formed on the photoresist. (*Id.*, col. 5, ll. 61-67.) Therefore, if one wished to prevent the hardened surface layer from being formed on the photoresist, the upper electrode should be grounded.

As such, the motivation provided by the Examiner to combine *Ikeda* and *Jiang* would result in a process that is modified by either or both of forming an upper electrode of silicon and/or connecting the upper electrode to ground. As such, the combination of *Ikeda* and *Jiang* (alone or modified by any of the cited references) fails to yield a plasma source power of at least about 1,000 W and a

bias power of at least about 800 W while etching during at least a portion of the etch step, as recited in claims 1 and 40.

In the Advisory Action dated November 22, 2005, the Examiner asserts that "the pointed to teachings of *Ikeda* do not negate the argument that *Ikeda* teaches the use of the recited bias power during at least a portion of the etch process… *i.e.*, the upper electrode would not be grounded during the entire etching step." This general assertion is restated in the Office Action dated February 24, 2006. However, the Applicants respectfully point out that the Examiner's rebuttal inappropriately presumes the combination. In other words, the Examiner is rebutting the argument that there is no motivation to combine the references in the manner suggested by stating that, if combined, the references would teach the limitations recited in the claims.

The initial burden lies on the Examiner to create a *prima facie* case of obviousness, which requires that some suggestion or motivation exists, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. In addition, the teaching or suggestion to make the claimed combination must be found in the prior art, and must not be based on the Applicant's disclosure. *MPEP* §2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

The requirement for providing a suggestion or motivation to combine the teachings of references is "rigorously applied" by the courts. (*In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); *see also*, *In re Kotzab*, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000)("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed")).

Examiners can satisfy this burden "only by showing some objective teaching in the prior art that would lead an individual to combine the relevant teachings of the references." (*In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992); *see also*, *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143 (Fed. Cir. 1985) (There must be some reason for the combination other than the hindsight gleaned from the invention itself to selectively combine prior art references to render a subsequent invention obvious.))

In the present case, the Examiner has not pointed to any "objective teaching" in *Ikeda* (or elsewhere) that would "lead an individual to combine the relevant teachings of the references." Specifically, as discussed above, *Ikeda* fails to provide any teaching, suggestion, or motivation to modify the teachings of *Jiang* with the plasma source and bias powers, as recited in claims 1 and 40, to obtain the benefit cited by the Examiner. The Examiner appears to be inadvertently and inappropriately using hindsight analysis to pick and choose teachings from the references to support the obviousness rejection. However, it is well-settled that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (*In re Fine*,837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)) Accordingly, the Applicants submit that the teachings of *Ikeda* cannot be combined with the remaining references in the manner suggested by the Examiner because there is no motivation or suggestion to do so.

In the Response to Amendment section of the Office Action dated February 24, 2006, the Examiner states that "the different mechanism to reduce F radicals in the process chamber of Ikeda… does not negate the provided step II in Ikeda's fig. 4." However, the Applicants respectfully point out that it is the "reduction in F radicals in the process chamber," that the Examiner is relying upon as motivation to combine *Ikeda* with *Jiang* and/or *Ma*. Hence, it is the "different mechanism" (*e.g.*, the silicon electrode discussed above) that provides the benefit asserted by the Examiner and not the process conditions stated in Figure 4 of *Ikeda*. As discussed above, *Ikeda* simply fails to provide a teaching,

suggestion, or motivation, to modify the teachings of *Jiang* and/or *Ma* to yield the limitations recited in either of claims 1 and 40.

Therefore, a *prima facie* case of obviousness has not been established because any permissible combination of the cited references fails to yield all of the limitations recited in each of independent claims 1 and 40, and all claims respectively depending therefrom. Specifically, the combination of the cited references fail to teach or suggest a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts during at least a portion of the etch step, as recited in claims 1 and 40. Moreover, a *prima facie* case of obviousness has further not been established because the is no suggestion or motivation to combine the cited references in the manner suggested by the Examiner.

Thus, independent claims 1 and 40, and claims 2-6, 8-10 and 41-45, respectively depending therefrom, are patentable over *Jiang* in view of *Ma* and/or *Ikeda*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

B. Claims 7

Claims 7, 11-17 and 44-45 stand rejected as being unpatentable over *Jiang* in view of *Ma* and/or *Ikeda*, as applied to claims 1-6, 8-10, and 40-45 above, and further in view of Taiwan Patent 544,815 published August 1, 2003 to *Chun, et al*. (hereinafter *Chun*), and United States Patent 6,177,147 issued on January 23, 2001 to *Samukawa, et al.* (hereinafter *Samukawa*). The Applicants respectfully disagree.

Independent claims 1 and 40, from which the rejected claims depend, recite limitations not taught or suggested by any combination of the cited art. The patentability of claims 1 and 40 over *Jiang* in view of *Ma* and/or *Ikeda* have been discussed above. *Chun* discloses a process for etching a nitride layer and an oxide layer using O_2, N_2, and CF_4 in a ratio of O_2:N_2:CF_4 equal to 4-50:0-10:1. *Chun* further discloses applying an RF power in the range of 100 to 1000 Watts but is silent regarding any bias power applied. (*Chun*, Abstract.) However, *Chun*

fails to teach or suggest a plasma source power of at least about 1,000 W and a bias power of at least about 800 W during at least a portion of the etch step, as recited in claims 1 and 40. As such, *Chun* fails to teach or suggest a modification of any combination of *Jiang*, *Ma*, and *Ikeda* that would yield the limitations recited in the claims.

Samukawa discloses a process and apparatus for treating a substrate using an ultra-high frequency (UHF) plasma. *Samukawa* further generally discloses applying a UHF RF power in the range of 0 to 1000 Watts but is silent regarding the bias power applied. (*Samukawa*, Figs 3, 6-8, and accompanying text.) However, *Samukawa* similarly fails to teach or suggest a plasma source power of at least about 1,000 W and a bias power of at least about 800 W during at least a portion of the etch step, as recited in claims 1 and 40. As such, *Samukawa* fails to teach or suggest a modification of any combination of *Jiang*, *Ma*, *Ikeda*, and *Chun* that would yield the limitations recited in the claims.

Therefore, a *prima facie* case of obviousness has not been established because any permissible combination of the cited references fails to yield all of the limitations recited in each of independent claims 1 and 40, and claims 7, 11-17, and 44-45, respectively depending therefrom. Specifically, the combination of the cited references fail to teach or suggest a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts during at least a portion of the etch step, as recited in claims 1 and 40. Moreover, a *prima facie* case of obviousness has further not been established because the is no suggestion or motivation to combine the cited references in the manner suggested by the Examiner.

Thus, independent claims 1 and 40, and claims 7, 11-17, and 44-45, respectively depending therefrom, are patentable over *Jiang* in view of *Ma* and/or *Ikeda*, and further in view of *Chun,* and *Samukawa*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Alan Taboada at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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